In the Specification:

On page 1, after the title, please amend the section entitled "Related Application" as follows:

RELATED APPLICATIONS

~~This application claims priority from Korean Application No. 2001-42355, filed July 13, 2001, the disclosure of which is hereby incorporated herein by reference.~~ This application claims priority to and is a divisional of parent application number 10/083,166, filed February 26, 2002, which claims the benefit of Korean Patent Application No. 2001-42355, filed July 13, 2001, the disclosures of which are hereby incorporated herein by reference.

Please amend the paragraph at page 9, lines14-29 as follows:

As shown in FIG. 3D, a second insulating layer 66 is also formed in, and at least partially filling, a space between the adjacent SEG layers 64 formed at the edges of and along the upper sidewall portions 56a of the trench 56. The second insulating layer 66 may be a polysilazane oxide layer having an associated fluidity. It will be understood that polysilazane typically has good gap-filling characteristics and superior tolerance of wet chemicals. Also, polysilazane generally has a high etching selectivity ~~fo~~ of SiN (8.3:1) and may be formed by a simple process. Polysilazane may be transformed into SiO_2 in a wet atmosphere, however, it is generally not transformed into SiO_2 in a wet or N_2 atmosphere. When a polysilazane oxide layer is used as the second insulating layer 66, the integrated circuit substrate 50 may be annealed at a predetermined temperature to increase the density of the second insulating layer 66. After annealing, the second insulating layer 66 may be etched back by wet or dry etching so that the surface of the SEG layer 64 is exposed and the trench 56 is filled with the first and second insulating layers 62 and 66. Thus, the present invention provides a method for implementing a shallow trench isolation (STI) region 70 in an integrated circuit device.